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Product Brief
April 2003

MARS1G2 T-LT (TSOT021G2) SONET/SDH 155/622 Mbits/s Overhead and Path Processor

Features

- One of the next generation system on a chip devices of Agere Systems' multiapplication & rate solutions *MARS*™ family of framers.
- Transmission convergence and SONET/SDH terminal/ADM functionality for linear and ring networks.
- Versatile IC supports 155/622 Mbits/s SONET/SDH overhead and path processor solutions.
- Low-power 1.6/3.3 V operation.

SONET/SDH Interface

- Termination of quad STS-3/STM-1 or dual STS-12/STM-4.
- Supports overhead processing for transport and path overhead bytes.
- Optional insertion and extraction of overhead bytes via serial overhead interface.
- STS pointer processing to align the receive frame to the system frame.
- STS-1 granularity cross connect between receive, mate, STM, and data payloads.
- Support for 1 + 1 and 1:1 linear networks; UPSR and BLSR ring networks.
- Full path termination and SPE extraction/insertion.
- SONET/SDH compliant condition and alarm reporting.
- Handles all concatenation levels of STS-3c to STS-24c (in multiples of 3: e.g., 3c, 6c, 9c, etc.).
- Built-in diagnostic loopback modes.
- Compliant with the following *Telcordia Technologies*®, *ANSI*®, and ITU standards:
  - — GR-253 CORE: SONET Transport Systems: Common Generic Criteria.
  - — ITU-T G.707: Network Node Interface for the Synchronous Digital Hierarchy.
  - — ITU-T G.803: Architecture of Transport Networks Based on the Synchronous Digital Hierarchy.
  - — T1.105: SONET-Basic Description including Multiplex Structure, Rates, and Formats.
  - — T1.105.02 SONET-Payload Mappings.
  - — T1.105.03 SONET-Jitter at Network Interfaces.
  - — T1.105.06 SONET Physical Layer Specifications.
  - — T1.105.07 SONET-Sub-STS-1 Interface Rates and Formats Specification.
  - — ITU-T I.432: B-ISDN User-Network Interface-Physical Layer Specification.
  - — IETF RFC 2615: PPP over SONET/SDH.
  - — IETF RFC 1661: The Point-to-Point Protocol (PPP).
  - — IETF RFC 1662: PPP in HDLC-like Framing.

Interfaces

- Built-in redundant STS/STM backplane interface using 622 MHz LVDS technology.
- Mate-to-mate backplane interface using 622 MHz LVDS technology for 1 + 1, 1:1, BLSR, and UPSR network support.
- Optional 78 MHz bus (32-bit) for STS/STM interface.
- *IEEE*® 1149.1 port with BIST, scan, and boundry scan.

Microprocessor Interface

- Up to 66 MHz synchronous.
- 16-bit address and 16-bit data interface.
- Synchronous or asynchronous modes available.
- Configurable to operate with most commercial microprocessors.

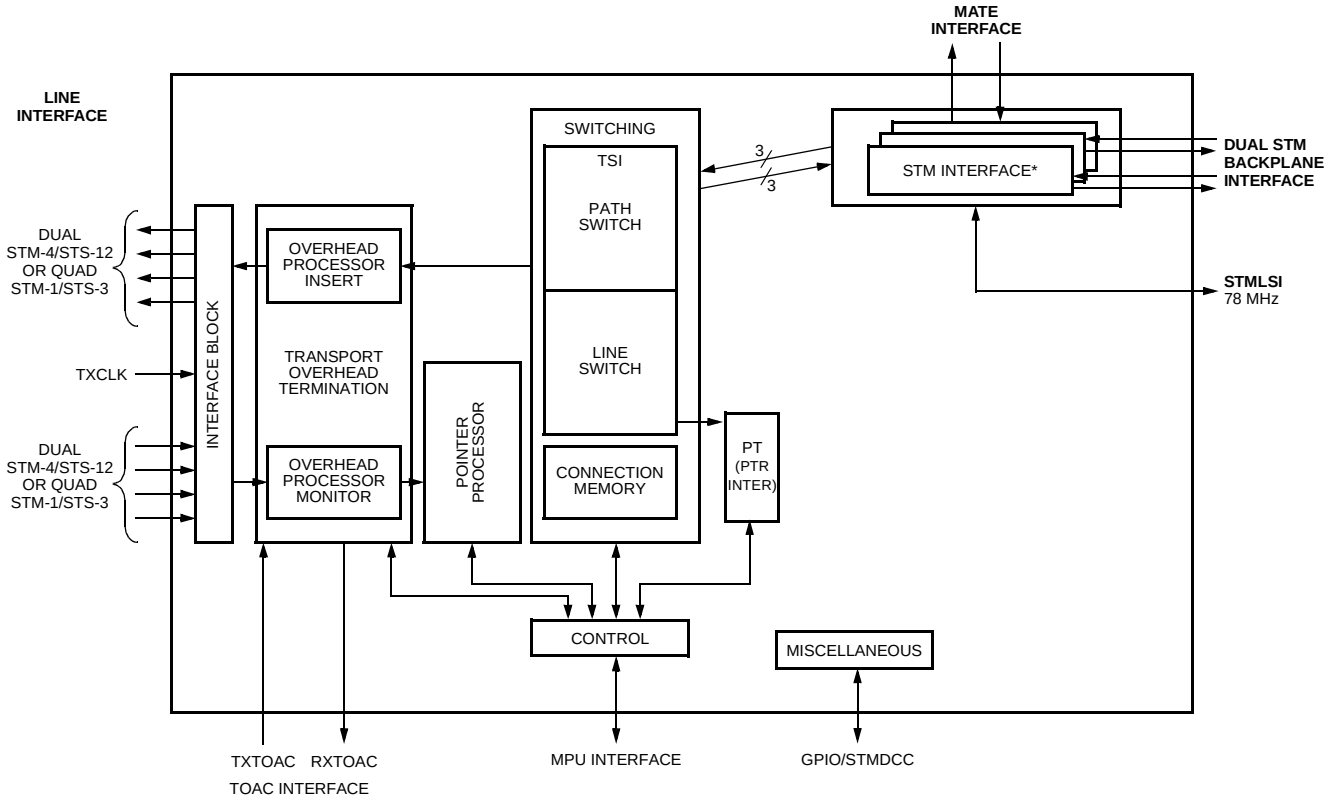
Description

The MARS1G2 T-LT SONET/SDH overhead and path processor provides a versatile solution for quad OC-3 and dual OC-12, linear and ring datacom/telecom applications. Constructed using COM2 CMOS modular process, this device incorporates integrated SONET/SDH section/line/path termination, pointer processing, and cross connect blocks.

Communication with the MARS1G2 T-LT device is accomplished through a generic microprocessor interface. The device supports separate address and data buses.

With this device, support for different types of applications for OC-3/OC-12 data equipment is possible, enabling dramatic system cost reduction and the ease of development of extremely competitive solutions.

The interface rates supported are dual STS-12/STM-4 and quad STS-3/STM-1. The concatenation levels supported by this device are STS-1, STS-3c, STS-6c, STS-9c, STS-12c, STS-15c, . . . , STS-21c, and STS-24c.



Note: PT = path terminator.

* An STM low-speed interface (STMLSI) is available.

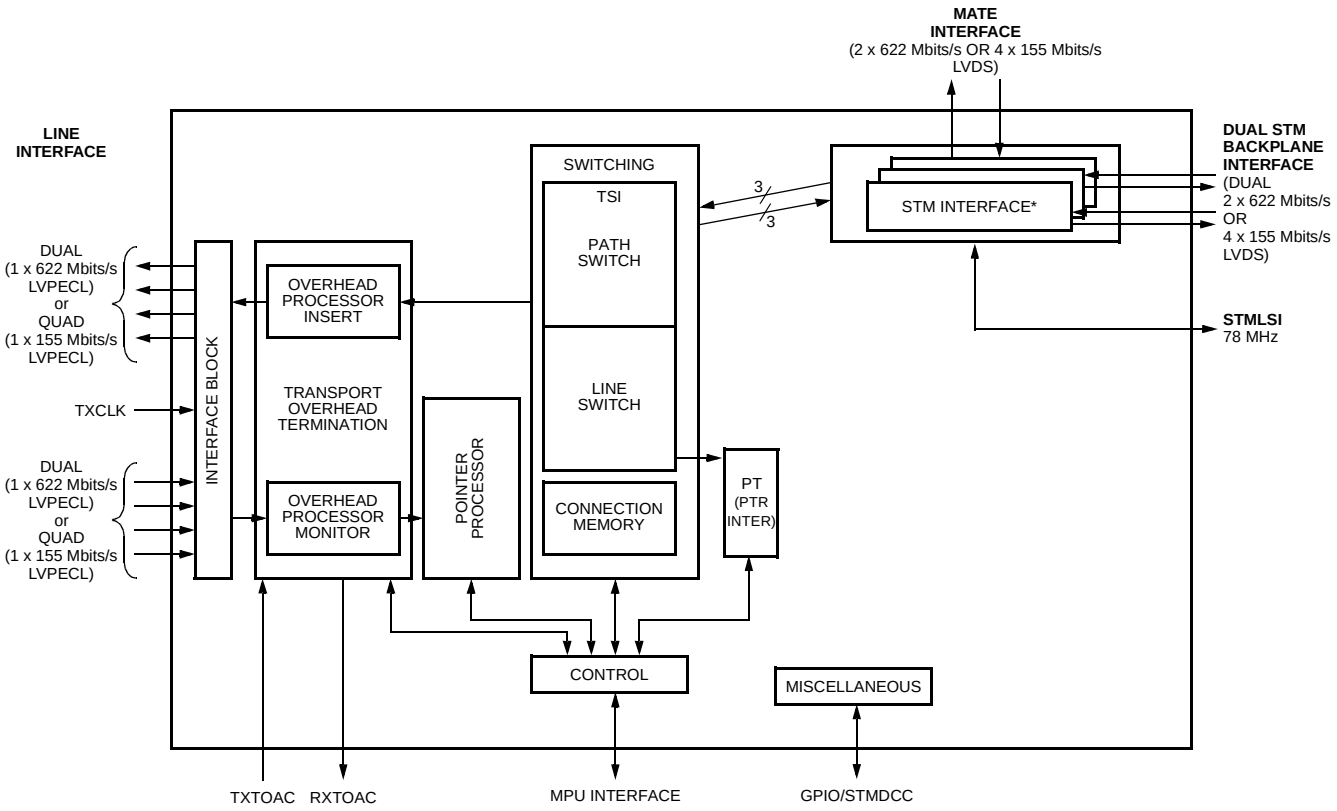
Figure 1. MARS1G2 T-LT Block Diagram

Target Applications Supported

MARS1G2 T-LT (792-Pin PBGA)

This multirate/multiprotocol/multimode SONET/SDH add/drop multiplexer device targets the following applications. See Figure 2 for device interface speed/rate information:

- PON.
- Access/core router.



* An STM low-speed interface (STMLSI) is available.

Figure 2. MARS1G2 T-LT Device Interface Speed/Rate Diagram

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April 2003
PB03-088SONT